#12
1-20-04

Our Docket No.: 042390.P9043

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Subramaniyam et al.

Application No.: 09/669,034

Filed: September 25, 2000

For: A CPU Power Management Mechanism

Examiner: Phan, Raymond Ngan

Art Group: 2181

APPEAL BRIEF
IN SUPPORT OF APPELLANT'S APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Appellant hereby submits this Brief in triplicate in support of its appeal from a final decision by the Examiner, mailed August 12, 2003, in the above-referenced Application. Appellant respectfully requests consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the above-captioned patent application.

An oral hearing is not desired.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision.

III. STATUS OF THE CLAIMS

Claims 1-24 are currently pending in the above-referenced application. In the Final Office Action mailed August 12, 2003, claims 1-3 and 8-24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hetherington et al. (U.S. Patent No. 5,978,864) ("*Hetherington*") in view of Shiell et al. (U.S. Patent No. 6,138,232) ("*Shiell*"). Further, claims 4-7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Hetherington* in view of *Shiell* and in further view of McFarland et al. (U.S. Patent No. 5,125,093) ("*McFarland*").

IV. STATUS OF AMENDMENTS

In response to the Final Office Action mailed on August 12, 2003, rejecting claims 1-24 under 35 U.S.C. §103(a), Appellant filed an After Final Response under 37 C.F.R §1.116. The Examiner mailed an Advisory Action on November 12, 2003. In response, Appellant filed a Notice of Appeal on November 19, 2003. A copy of all claims on appeal is attached hereto as an Appendix of Claims.

V. SUMMARY OF THE INVENTION

According to one embodiment, a system is described. The system includes a central processing unit (CPU) including power management logic to enable the CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold.

In another embodiment, a method is disclosed. The method includes determining whether the temperature of a CPU exceeds a predetermined threshold, executing a first quantity of instructions per cycle if the temperature of the CPU exceeds the predetermined threshold, and executing a second quantity of instructions per cycle if the temperature of the CPU is below the predetermined threshold.

In yet another embodiment, a CPU includes a thermal sensor, and an instruction execution unit to generate a first quantity of instructions per cycle in a first execution mode whenever the thermal sensor measures temperature exceeding a predetermined threshold and to generate a second quantity of instructions per cycle in a second execution mode whenever the thermal sensor measures temperature below the predetermined threshold.

In a further embodiment, power management logic includes a thermal sensor, and an instruction execution unit to generate a first quantity of instructions per cycle in a first execution mode whenever the thermal sensor measures a temperature exceeding a predetermined threshold and to generate a second quantity of instructions per cycle in a second execution mode whenever the thermal sensor measures temperature below the predetermined threshold. In addition, the power management logic includes interrupt generating hardware to generate a first interrupt whenever the thermal sensor measures a

temperature that exceeds the predetermined threshold and generates a second interrupt whenever the thermal sensor measures a temperature below the predetermined threshold.

VI. ISSUES PRESENTED

Whether claims 1-3 and 8-24 are patentable over *Hetherington* in view of *Shiell* under 35 U.S.C. §103(a); and

Whether claims 4-7 are patentable over *Hetherington* and *Shiell* in view of *McFarland* under U.S.C. §103(a).

VII. GROUPING OF CLAIMS

For the purposes of this appeal, claims 1-24 stand or fall together as Group I.

VIII. ARGUMENT

1. Claim Group I

A.

THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 103(A) BECAUSE NEITHER *HETHERINGTON* NOR *SHIELL* DISCLOSE OR SUGGEST A CPU TO EXECUTE A FIRST QUANTITY OF INSTRUCTIONS PER CYCLE WHENEVER THE TEMPERATURE OF THE CPU EXCEEDS A PREDETERMINED THRESHOLD AND TO EXECUTE A SECOND QUANTITY OF INSTRUCTIONS PER CYCLE WHENEVER THE TEMPERATURE OF THE CPU IS BELOW THE PREDETERMINED THRESHOLD

Appellant respectfully submits that the claims in Claim Group I are not obvious in view of *Hetherington* and *Shiell* for the reasons set forth below.

Each claim in Claim Group I recites an element that is not disclosed or suggested in *Hetherington* or *Shiell*. For example, Appellant's claim 1 recites the following:

> A system comprising a central processing unit (CPU) including power management logic to enable the CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold.

Appellant's claim 8 recites:

> A method comprising:
> determining whether the temperature of a central processing unit (CPU) exceeds a predetermined threshold;
> executing a first quantity of instructions per cycle if the temperature of the CPU exceeds the predetermined threshold; and
> executing a second quantity of instructions per cycle if the temperature of the CPU is below the predetermined threshold.

Appellant's claim 16 recites:

> A central processing unit (CPU) comprising:
> a thermal sensor; and
> an instruction execution unit to generate a first quantity of instructions per cycle in a first execution mode whenever the thermal sensor measures temperature exceeding a predetermined threshold and to generate a second quantity of instructions per cycle in a second execution mode whenever the thermal sensor measures temperature below the predetermined threshold.

Appellant's claim 20 recites:

> Power management logic comprising:
> a thermal sensor; and
> an instruction execution unit to generate a first quantity of instructions per cycle in a first execution mode whenever the thermal sensor measures a temperature exceeding a predetermined threshold and to generate a second quantity of instructions per cycle in a second execution mode whenever the thermal sensor measures temperature below the predetermined threshold; and
> interrupt generating hardware to generate a first interrupt whenever the thermal sensor measures a temperature that exceeds the predetermined threshold and generates a second interrupt whenever the thermal sensor measures a temperature below the predetermined threshold.

Hetherington discloses a system and method for thermal overload detection and protection for an integrated circuit processor. The system allows the processor to run at near maximum potential for the vast majority of its execution life. This is effectuated by the provision of circuitry to detect when the processor has exceeded its thermal thresholds and which then causes the processor to automatically reduce the clock rate to a fraction of the nominal clock while execution continues. When the thermal condition has stabilized, the clock may be raised in a stepwise fashion back to the nominal clock rate. See *Hetherington* at col. 3, ll. 53-65.

Further, the system discloses a thermal sensing circuit that incorporates a programmable threshold which, when reached, causes the circuit to generate a non-masked interrupt to the processor which may be identical to a power down "Energy Star" interrupt. The internal phase-locked loop ("PLL") clock dividers may be employed to step down the master clock from nominal to, for example, 1/64th of the nominal rate. Program execution would then continue at this lowered or reduced clock rate until the thermal sensing circuit again senses that a temperature threshold has been crossed, whereupon it may again issue a non-masked interrupt to raise the clock back to nominal frequency. As before, normal program execution commences at the conclusion of the interrupt (col. 4, ll. 42-58).

Shiell discloses a method of operating a microprocessor. The microprocessor accepts an interrupt from one of a plurality of interrupt sources. The microprocessor then operates at a rate dependent upon the interrupt source. The rate of power consumption by the microprocessor corresponds to the selected rate of instruction operation. A rate table stores a table of interrupt source to rate of instruction operation. The rate table is accessed upon receipt of an interrupt to obtain a rate of instruction operation corresponding to the interrupt source. The microprocessor is then operated at the recalled rate. The rate table may be a read only memory or a read/write memory loaded upon initiation of the microprocessor. The rate of instruction operation may be controlled by a rate of instruction dispatch. For a superscalar microprocessor capable of concurrently executing plural instructions simultaneously the rate of instruction operation may be set by setting a number of instructions dispatched per instruction cycle. This could include dispatching instructions to a number of execution units based upon the selected rate. Electric power consumption is conserved by powering only those execution units to which instructions are dispatched. See *Shiell* at col. 1, ll. 45 – col. 2, ll. 25.

Appellant submits that neither *Hetherington* nor *Shiell* disclose or suggest a CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU

exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold. As discussed above, *Hetherington* discloses circuitry to detect when a processor has exceeded its thermal thresholds, and in response causes the processor to automatically reduce a clock rate to a fraction of a nominal clock while execution continues. When the thermal condition has stabilized, the clock may be raised in a stepwise fashion back to the nominal clock rate. Meanwhile, *Shiell* discloses a microprocessor receiving an interrupt and operating at a rate dependent upon an interrupt source.

Therefore, *Hetherington* and *Shiell* do not disclose or suggest a CPU to execute a first quantity of instructions per cycle whenever a temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold. Because neither *Hetherington* nor *Shiell* disclose or suggest a CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold, any combination of *Hetherington* and *Shiell* would also not disclose or suggest such a limitation.

Moreover, it is also respectfully submitted that *Hetherington* does not teach or suggest a combination with *Shiell* and that *Shiell* does not teach or suggest a combination with *Hetherington*. As previously described, *Hetherington* includes a circuit that reduces processor power by reducing the processor clock rate to a fraction of the normal rate. Meanwhile, *Shiell* discloses a mechanism to service interrupts in a processor and operating at a rate dependent of an interrupt source. Therefore, Appellant submits that it would be impermissible hindsight based Appellant 's own disclosure to incorporate the *Shiell* interrupt service mechanism into *Hetherington's* thermal overload detection and prevention mechanism. Furthermore, such a combination would still not disclose or suggest a CPU to execute a first quantity of instructions per cycle whenever the

temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold.

For the foregoing reasons, Appellant submits that the Examiner has failed to establish a *prima facie* case of obviousness as set forth in MPEP § 706.02(j). Specifically, the Examiner has failed to show that "[t]he teaching or suggestion to make the claimed combination ... [is] found in the prior art, and not based on Appellant's disclosure," as required by In re Vaeck, 947 F.2d 488 (Fed. Cir. 1991).

Claims 2-7, 9-15, 17-19 and 21-24 depend from claims 1, 8, 16 and 20, respectively. Given that dependent claims necessarily include the limitations of the claims from which they depend, Appellant submits that the invention as claimed in claims 2-7, 9-15, 17-19 and 21-24 are similarly also patentable in view of *Hetherington* and *Shiell*.

Thus, the Examiner erred in rejecting claims 1-3 and 8-24 under 35 U.S.C. § 103(a) in view of *Hetherington* and *Shiell*.

B.

THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 103(A) BECAUSE NEITHER *HETHERINGTON, SHIELL* NOR *MCFARLAND* DISCLOSE OR SUGGEST A CPU TO EXECUTE A FIRST QUANTITY OF INSTRUCTIONS PER CYCLE WHENEVER THE TEMPERATURE OF THE CPU EXCEEDS A PREDETERMINED THRESHOLD AND TO EXECUTE A SECOND QUANTITY OF INSTRUCTIONS PER CYCLE WHENEVER THE TEMPERATURE OF THE CPU IS BELOW THE PREDETERMINED THRESHOLD

Appellant respectfully submits that the claims in Claim Group I are not obvious in view of the combination of *Hetherington*, *Shiell* and *McFarland* for the reasons set forth below.

McFarland discloses a technique of servicing interrupts among a plurality of microprocessors. See *McFarland* at Abstract. Nevertheless, *McFarland* does not disclose or suggest a CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold.

As described above, neither *Hetherington* nor *Shiell* disclose or suggest such a limitation. Therefore, any combination of *Hetherington*, *Shiell* and *McFarland* would also not disclose or suggest a CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold.

For the foregoing reasons, Appellant submits that the Examiner has failed to establish a *prima facie* case of obviousness as set forth in MPEP § 706.02(j). Specifically, the Examiner has failed to show that "[t]he teaching or suggestion to make

the claimed combination ... [is] found in the prior art, and not based on Appellant's disclosure," as required by In re Vaeck, 947 F.2d 488 (Fed. Cir. 1991).

Thus, the Examiner erred in rejecting claims 4-7 under 35 U.S.C. § 103(a) in view of *Hetherington*, *Shiell* and *McFarland*.

IX. CONCLUSION

Careful review of the Examiner's rejections shows that the Examiner has failed to provide any reference, or combination of references of the prior art that shows all of the elements of each appealed claim. Therefore, Appellant respectfully submits that all appealed claims in this application are patentable and were improperly rejected by the Examiner during prosecution before the United States Patent and Trademark Office. Appellant respectfully requests that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

This brief is submitted in triplicate, along with a check for $330.00 to cover the appeal fee for one other than a small entity as specified in 37 C.F.R. § 1.17(c). Please charge any shortages and credit any overcharges to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: January 8, 2004

Mark L. Watson
Reg. No. 46,322

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA. 90025-1026
(408) 720-8598

X. APPENDIX OF CLAIMS (37 C.F.R. § 1.192(c)(9))

The claims on appeal read as follows:

1. A system comprising a central processing unit (CPU) including power management logic to enable the CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold.

2. The system of claim 1 wherein the power management logic comprises:

a thermal sensor;

a digital filter coupled to the thermal sensor; and

an interrupt generating hardware coupled to the digital filter, wherein the interrupt generating hardware generates a first interrupt whenever the temperature of the CPU exceeds the predetermined threshold and generates a second interrupt whenever the temperature of the CPU is below the predetermined threshold.

3. The system of claim 2 wherein the power management logic further comprises an analog to digital converter coupled between the thermal sensor and the digital filter.

4. The system of claim 2 further comprising programmable array logic (PAL), wherein the PAL includes an interrupt handler for receiving the first and second interrupts.

5. The system of claim 4 wherein the power management logic further comprises:

an instruction execution unit coupled to the interrupt handler; and

an artificial activity generator coupled to the interrupt handler.

6. The system of claim 5 wherein the instruction execution unit executes six instructions per cycle in the first execution mode whenever the die temperature is below the predetermined threshold temperature and executes one instruction per cycle in the second execution whenever the die temperature is above the predetermined threshold temperature.

7. The system of claim 5 wherein the artificial activity generator causes the CPU artificial activity generator to suspend artificial activity within the CPU whenever the die temperature is above the predetermined threshold temperature.

8. A method comprising:

determining whether the temperature of a central processing unit (CPU) exceeds a predetermined threshold;

executing a first quantity of instructions per cycle if the temperature of the CPU exceeds the predetermined threshold; and

executing a second quantity of instructions per cycle if the temperature of the CPU is below the predetermined threshold.

9. The method of claim 8 further comprising:

generating a first interrupt if the temperature of the CPU exceeds the predetermined threshold;

interrupting an artificial activity mode; and

transitioning from a full instruction execution mode to a single instruction execution mode.

10. The method of claim 9 further comprising:

suspending the execution of code at the CPU after generating the first interrupt; and

resuming the execution of code at the CPU after transitioning to the single instruction execution mode.

11. The method of claim 10 further comprising:

determining whether the temperature of the CPU exceeds the predetermined threshold after transitioning to the single instruction execution mode; and

terminating the operation of the CPU if the temperature of the CPU exceeds the predetermined threshold after transitioning to the single instruction execution mode.

12. The method of claim 10 further comprising:

determining whether the temperature of the CPU exceeds the predetermined threshold after transitioning to the single instruction execution mode; and

generating a second interrupt if the CPU does not exceed the predetermined threshold after transitioning to the single instruction execution mode.

13. The method of claim 12 further comprising transitioning from the second execution mode to the first execution mode.

14. The method of claim 13 wherein the process of transitioning from the second execution mode to the first execution mode comprises:

resuming the artificial activity mode; and

transitioning from the single instruction execution mode to the full instruction execution mode.

15. The method of claim 12 wherein the first interrupt is a high temperature interrupt and the second interrupt is a normal temperature interrupt.

16. A central processing unit (CPU) comprising:

a thermal sensor; and

an instruction execution unit to generate a first quantity of instructions per cycle in a first execution mode whenever the thermal sensor measures temperature exceeding a predetermined threshold and to generate a second quantity of instructions per cycle in a second execution mode whenever the thermal sensor measures temperature below the predetermined threshold.

17. The CPU of claim 16 further comprising:

interrupt generating hardware coupled to generate a first interrupt whenever the thermal sensor measures a temperature that exceeds the predetermined threshold and generates a second interrupt whenever the thermal sensor measures a temperature below the predetermined threshold.

18. The CPU of claim 17 further comprising an artificial activity generator.

19. The CPU of claim 18 wherein the artificial activity generator causes the artificial activity generator to suspend artificial activity within the CPU whenever the die temperature is above the predetermined threshold temperature.

20. Power management logic comprising:

a thermal sensor; and

an instruction execution unit to generate a first quantity of instructions per cycle in a first execution mode whenever the thermal sensor measures a temperature exceeding

a predetermined threshold and to generate a second quantity of instructions per cycle in a second execution mode whenever the thermal sensor measures temperature below the predetermined threshold; and

interrupt generating hardware to generate a first interrupt whenever the thermal sensor measures a temperature that exceeds the predetermined threshold and generates a second interrupt whenever the thermal sensor measures a temperature below the predetermined threshold.

21. The power management logic of claim 20 further comprising:

an analog to digital converter coupled to the thermal sensor.

22. The power management logic of claim 20 further comprising an artificial activity generator.

23. The power management logic of claim 22 wherein the artificial activity generator causes the artificial activity generator to suspend artificial activity within the CPU whenever the die temperature is above the predetermined threshold temperature.

24. The power management logic of claim 21 further comprising:

a digital filter coupled to the analog to digital converter and the interrupt generating hardware.